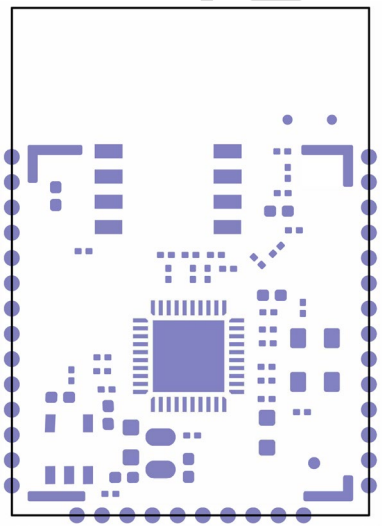
EWN-8720CMN1AA

Datasheet V1.0

Wi-Fi&BT Module



APPROVAL
L Y K
2022/01/18

Contents

1 General Specifications

EWN-8720CMN1AA is a highly integrated module with a low power 802.11n Wireless LAN compatible network controller. It combine a Real-M300(KM4) CPU that is based on ARMv8-M architecture, and carry WLAN MAC, a 1T1R capable WLAN baseband, an RF circuit, and Bluetooth Low Energy(BLE) in a single chip.

2 Features

MCU Features

- Real-M300(KM4) clock frequency up to 100MHz
- I-Cache 32KB/D-Cache 16KB
- Supports DMA
- EXecute In Place (XIP) on flash

Internal Memory

- Supports 384KB ROM
- Supports 256KB RAM
- Supports external flash interface
- Supports MCM embedded 4MB Psram
- Supports 2Mbit~32Mbit Flash

Wi-Fi Features

- 2.4GHz 802.11 b/g/n
- Support low power Tx/Rx for short-range application
- Support WPA/WPA2/ WMM/WPS
- Frame aggregation for increased MAC efficiency
- Low latency immediate High-Throughput Block Acknowledgement
- Long NAV for media reservation with CF-End for NAV release

Bluetooth Low Energy

- Bluetooth Low Energy(BLE) 4.2
- Supports LE secure connections/LE scatternet
- Supports 1 Master/1 Slave

Secure

- Supports secure boot
- Wi-Fi WEP, WPA, WPA2, WPS
- MD5/SHA-1/SHA2-224/SHA2-256/HMAC/AES Crypto engine

Interface

- SPI/SDIO/UART interface
- SPI/I2C master for sensor
- I2S, PWM and GPIO
- 1 GDMA with 2 channels

3 System Block Diagram

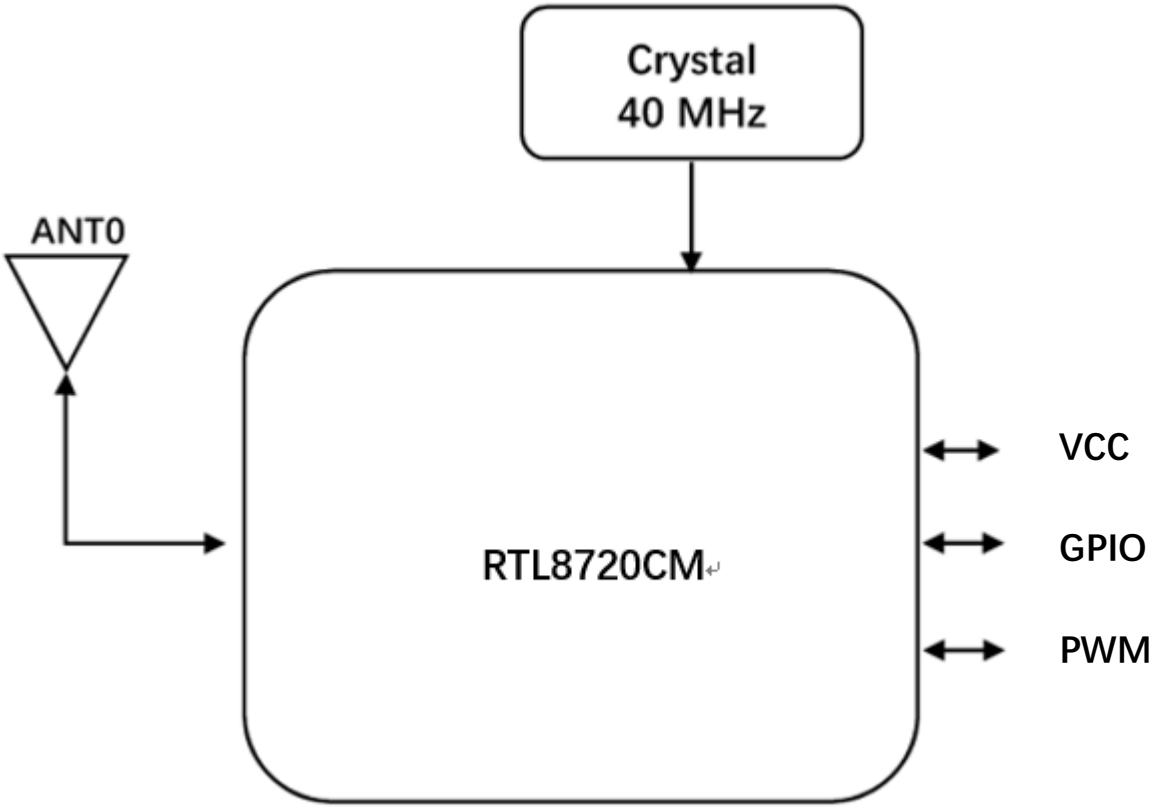


Fig 1 System Block Diagram

4 PHY Specification

Table 1 Wi-Fi RF Parameters

Protocol	IEEE 802.11b/g/n
Interface	UART
Frequency	2.4GHz band CH1~CH13/2412~2484MHz
Bandwidth	20M
2.4G Transmit Power	802.11b (2.4G 11M): 16±2dBm @ EVM <-15dB; 802.11g (2.4G 54M): 15±2dBm @ EVM <-25dB; 802.11n (2.4G HT20 MCS7): 13±2dBm @ EVM <-28dB;
Frequency Error	<±10ppm/802.11b/g/n
Mask	-20dB/±11MHz/OFDM;
	-28dB/±20MHz/OFDM;
	-30dB/±11MHz/DSSS, CCK;
2.4G Receive Sensitivity @ PER<10%	802.11b (2.4G 1M): -97dBm, typical; 802.11b (2.4G 11M): -88dBm, typical; 802.11g (2.4G 6M): -92.5dBm, typical; 802.11g (2.4G 54M): -74.5dBm, typical; 802.11n (2.4G HT20 MCS0): -92dBm, typical; 802.11n (2.4G HT20 MCS7): -72.5dBm, typical;

Table 2 Bluetooth RF Parameters

Protocol	BLE v4.2
Frequency	2402 MHz ~ 2480 MHz
Transmit Power	4dBm, typical
Frequency Error	<±20ppm

5 Other Specifications

Table 3 other Specifications

Operating Temperature	-40℃~+85℃
Storage Temperature	Module: -40℃~+85℃ Package: -20℃~+70℃
Operating Humidity	RH 95%(Non-Condensing)
Storage Humidity	RH 95%(Non-Condensing)
Humidity level	Level 3
Security	WPA,WPA2,WEP

6 DC Specifications

Table 4 DC Specifications

Item	Sym.	Min.	Typ.	Max.	Unit
VDD_3.3V	V_{BAT}	3	3.3	3.6	V

7 Module configurations

Module Size (Unit: mm): 18.0(±0.2) *25.50(±0.3)*2.9(±0.2)

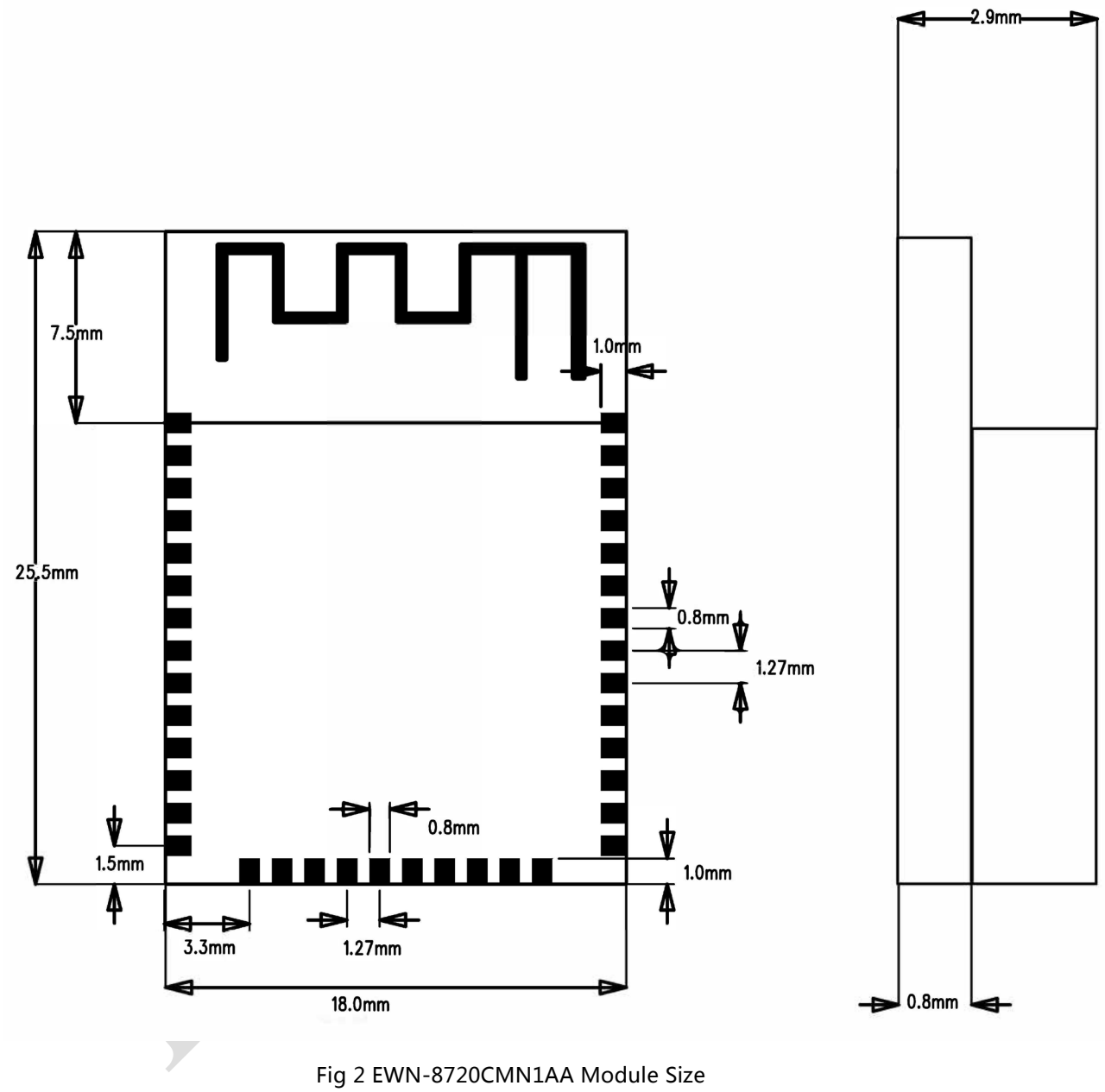


Fig 2 EWN-8720CMN1AA Module Size

8 Pin Definition

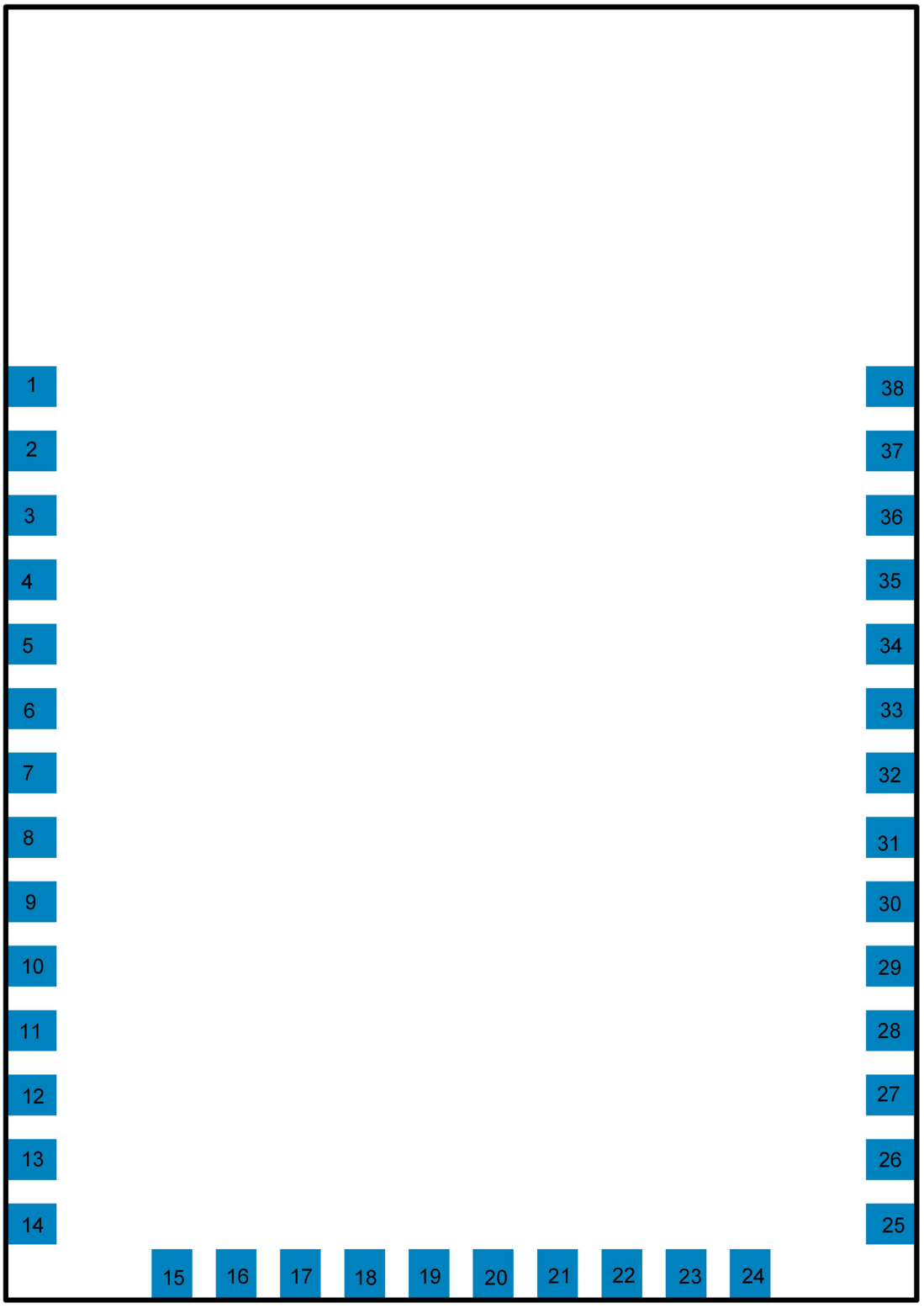


Fig 3 Top view

Table 5 the hardware Pin definition of the module

Table 5 Pin definition

PIN	Definition	Description
1	GND	Ground
2	VCC	Supply power 3.3V；
3	CHIP_EN	1:Enable chip 2:Shutdown chip
4	GPIOA_0 (TEST_MODE_SEL)	JTAG_CLK/UART1_IN/PWM[0] 1:Enter into test/debug mode 0:Normal operation mode
5	GPIOA_1 (Autoload_Fail)	JTAG_TMS/UART1_OUT/PWM[1] 1:eFUSE settings are not loaded 2:eFUSE settings are loaded
6	GPIOA_2	JTAG_TDO/UART1_IN/PWM[2]/SPI_CSn/I2C_SCL
7	GPIOA_3	JTAG_TDI/UART1_OUT/PWM[3]/SPI_SCL/I2C_SDA
8	GPIOA_4	JTAG_TRST/UART1_CTS/PWM[4]/SPI_MOSI
9	GPIOA_7	Flash_SPI_CS/SPI_M_CS/SPI_CSn
10	GPIOA_8	Flash _SPI_CLK/SPI_M_CLK/SPI_SCL
11	GPIOA_9	Flash _SPI_WP/SPI_M_DATA[2]/SPI_MOSI/UART0_RTS
12	GPIOA_10	Flash _SPI_SO/SPI_M_DATA[1]/SPI_MISO/UART0_CTS
13	GPIOA_11	Flash _SPI_SI/SPI_M_DATA[0]/I2C_SCL/UART0_OUT/PWM[0]
14	GPIOA_12	Flash _SPI_HOLD/SPI_M_DATA[3]/I2C_SDA/UART0_IN/PWM[1]
15	GND	Ground
16	GPIOA_13	UART0_IN/PWM[7]
17	GPIOA_14	SDIO_INT/UART0_OUT/PWM[2]
18	GPIOA_15	SDIO_D[2]/UART2_IN/PWM[3]/SPI_CSn/I2C_SCL
19	GPIOA_16	SDIO_D[3]/UART2_OUT/PWM[4]/SPI_SCL/I2C_SDA
20	GPIOA_17	SDIO_CMD/ PWM[5]
21	GPIOA_18	SDIO_CLK/ PWM[6]
22	GPIOA_19	SDIO_D[0]/UART2_CTS/PWM[7]/SPI_MOSI/I2C_SCL
23	GPIOA_20	SDIO_D[1]/UART2_RTS/PWM[0]/SPI_MISO/I2C_SDA

PIN	Definition	Description
27	GPIOA_23	LED_0/PWM[7]
38	GND	Ground

Notes:

1、UART download：Using A15&A16, and before power on.

2、Default states of all pins are High-impedance; Unused pins should be kept floating.

3、Some IO are used to connect to the flash of the module. It is recommended not to use these IO. As shown in the table.

Table 6 Flash definition

PIN	Definition	Description
9	GPIOA_7	Flash_SPI_CS
10	GPIOA_8	Flash _SPI_CLK
11	GPIOA_9	Flash _SPI_WP
12	GPIOA_10	Flash _SPI_SO
13	GPIOA_11	Flash _SPI_SI
14	GPIOA_12	Flash _SPI_HOLD

9 Module Photos

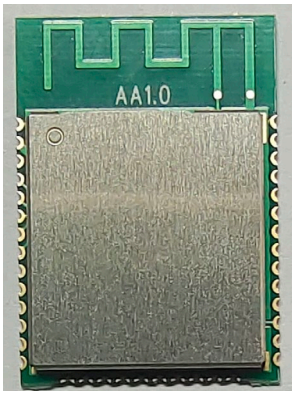


Fig 4 Top View

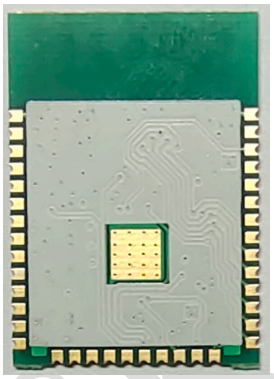


Fig 5 Bottom View

10 Key material list

Table 7 Key material list

Type	Model	Footprint	QTY.
Crystal	40MHz 9pF	3225	1PCS
IC	RTL8720CM	QFN40	1PCS

11 Reference design

11.1 RF

a) Under the antenna and in the two directions indicated by the arrow, avoid covering the ground, routing and placing metal components. It is better to directly hollow out the PCB in this area.

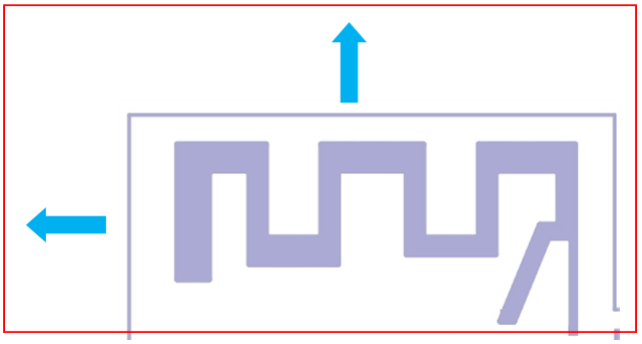


Fig 6 Antenna

b) It is recommended not to use any components within 30mm of the module antenna area, and the module baseboard should also avoid wiring and covering the ground as much as possible.

c) It is strongly recommended that the user place the antenna of the Bluetooth module close to the edge of the backplane as far as possible when laying out the PCB, as shown in the figure below, so as to ensure the good performance of the antenna.

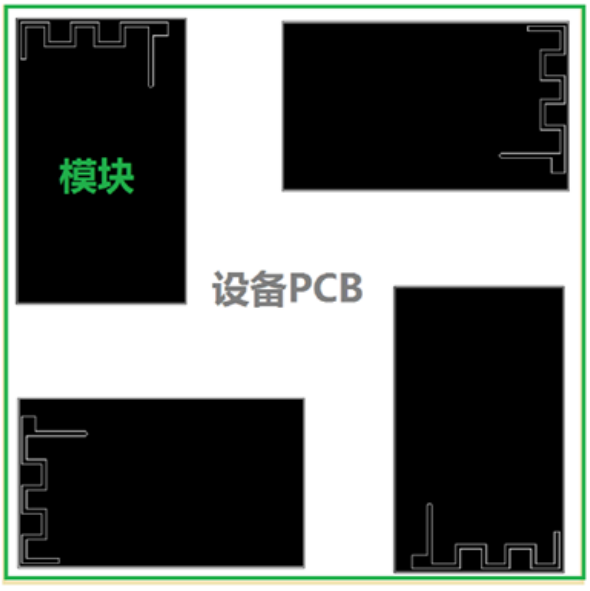


Fig 7 Recommended PCB layout

11.2 Power supply requirement

The module power supply voltage is DC+3.3V. The power supply design needs to consider the output current and power interference. The power supply current design needs to reserve 300mA. To avoid the +3.3V power supply from interfering with other circuits on the motherboard, it is recommended to supply to the module using the regulator circuit alone. the recommended DC-DC circuit structure shown in the figure below. A 4.7uF~10uF capacitor is connected in parallel at 3_3VD output to filter out the interference. A bead is connected in series at 3_3VD output. The bead and capacitor must be placed as close to the module as possible. If you need to share +3.3V with other circuits, consider whether the current of the shared power supply is sufficient.

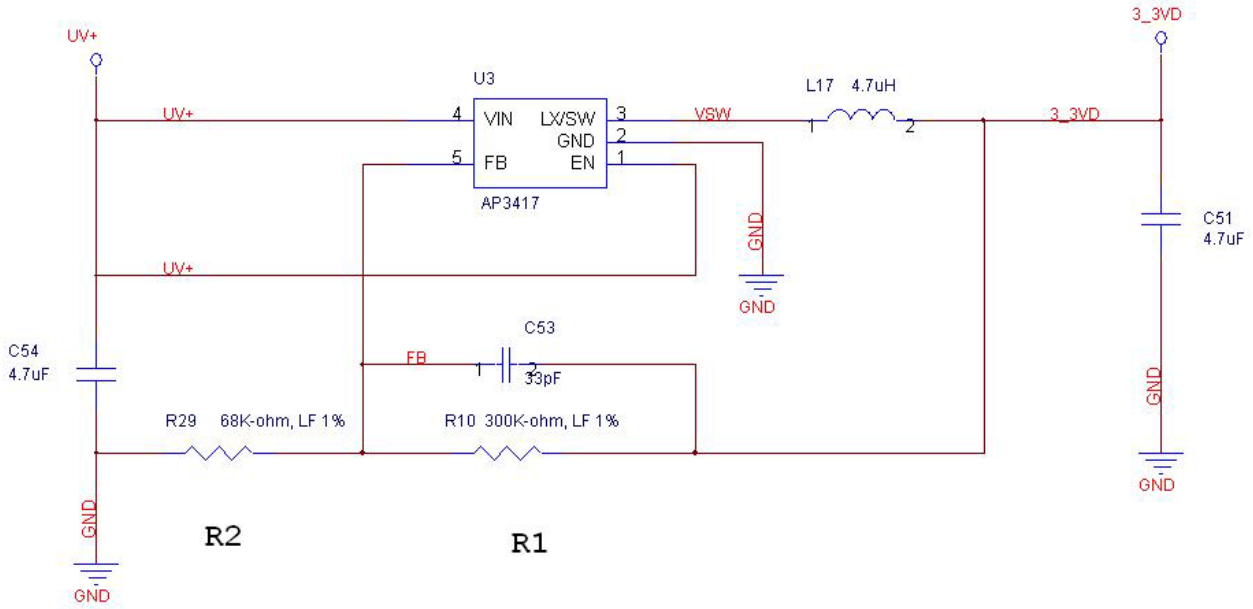


Fig 8 Power supply Circuit schematic

11.3 Motherboard interference avoidance

Motherboard interference comes from: high-speed data interface (HDMI), the Operating frequency of main chip, DDR, DC-DC power supply. The method of avoiding interference according to the characteristics of various signals is also different. The main methods of interference avoidance include:

1. keeping away from the source of interference;

2. Adding shields to avoid interference leakage;

3. Reasonable layout to eliminate interference.

11.3.1 Interface interference

When HDMI uses the 74.2MHz frequency, its 33x frequency is in the 2.4G band of BT, which will seriously interfere with the BT signal. If the HDMI frequency is 148.5MHz, although the 16x frequency is not in the BT band, the isolation of the frequency is not good, and the BT signal will be interfered to some extent. If the distance between the HDMI interface and the BT module on the PCB is less than 5cm, the HDMI output display will interfere with the BT signal, resulting in problems such as BT connection failure and throughput drop. Therefore, keep the location of the BT module away from the HDMI port on the hardware layout to avoid interference.

At the same time, if the BT antenna is built-in the motherboard, its placement must also be carefully considered to be far from the interface interference. If the antenna is placed in an incorrect position, even if the module is shielded, the interference signal is coupled through the antenna, which will eventually result in a lower BT throughput. (Note: In addition to interference, the placement of the internal antenna should also evaluate the effect of the metal interface, motherboard, and housing material on the antenna impedance.)

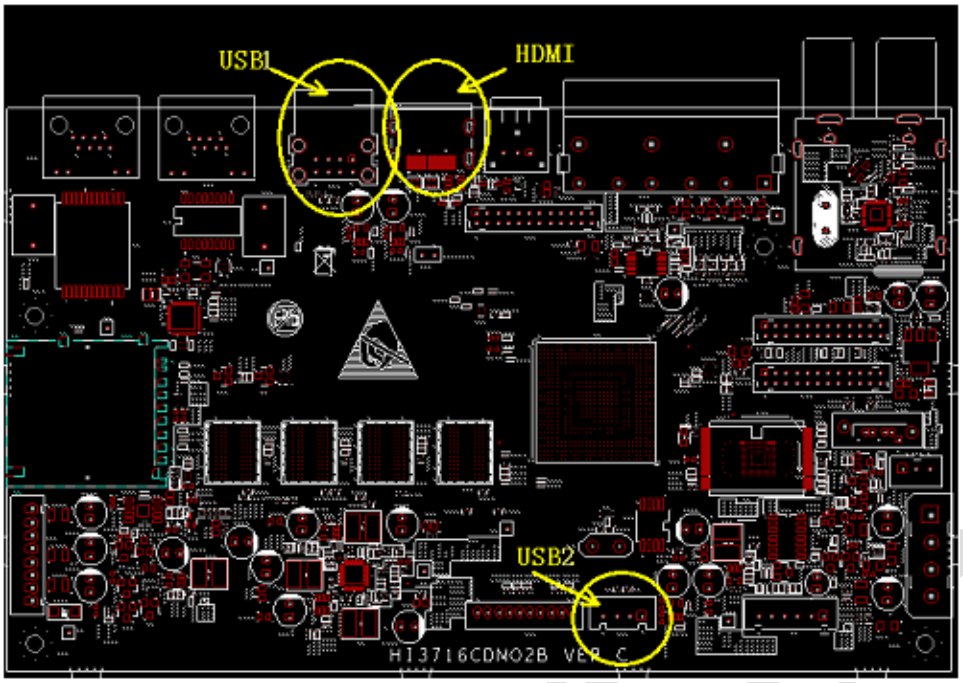


Fig 9 HDIM and USB interference

11.3.2 The main chip interferes with DDR

Because the main chips operate at about 800MHz or DDR2 operate at 667MHz, 3x frequency of 800MHz and 4x frequency of 667MHz are near 2.4GHz band. It must to place BT modules and antennas far away from the main chip and DDR. It is strongly recommended that the main chip be isolated from the DDR by a shield. As shown in the figure below.

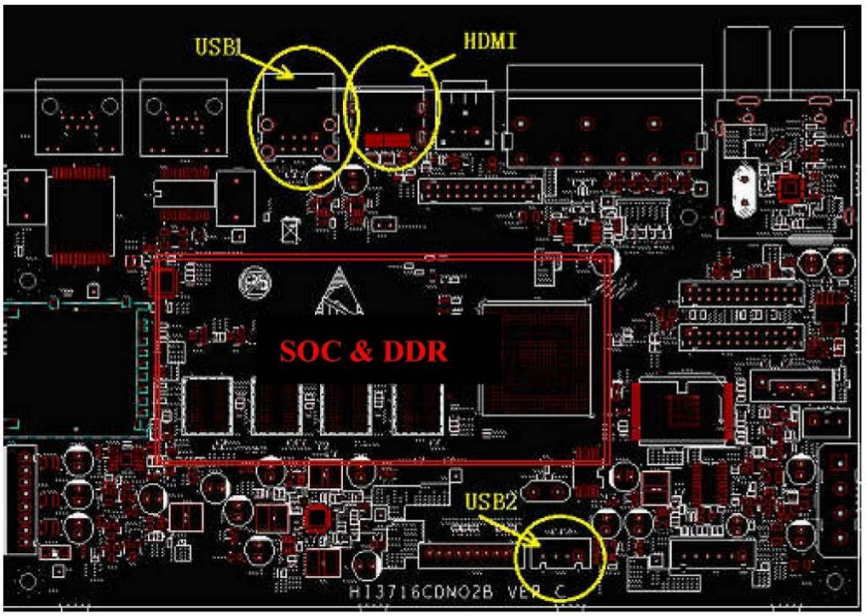


Fig 10 Main chip and DDR interference

11.4 Recommended secondary reflux temperature curve

T he number of reflux shall not exceed 2 times, and the tin feeding height of the half hole of the module shall be no less than 1/4.

The lead-free reflux curve requirements of BT module products are shown in figure 11：

Stage	Note	Pb-free assembly
Average ramp-up rate	T_L to Tp	3 ℃/ second max.
Preheat	Temperature min (T_{smin})	150℃
	Temperature max (Tsmax)	200℃
	Time (t_{smin} to t_{smax})	60 – 120 seconds
Time maintained above	Temperature(T_L)	217℃
	Time (t_L)	60 – 150 seconds
Peak package body temperature (Tp)		Tp must not exceed the specified classification temp(Tc=245℃).
Time(tp) within 5℃ of the specified classification temperature (Tc)		30 seconds
Ramp-down rate (Tp to T_L)		6 ℃ / seconds max.
Time 25℃ to peak temperature		8 minutes max.

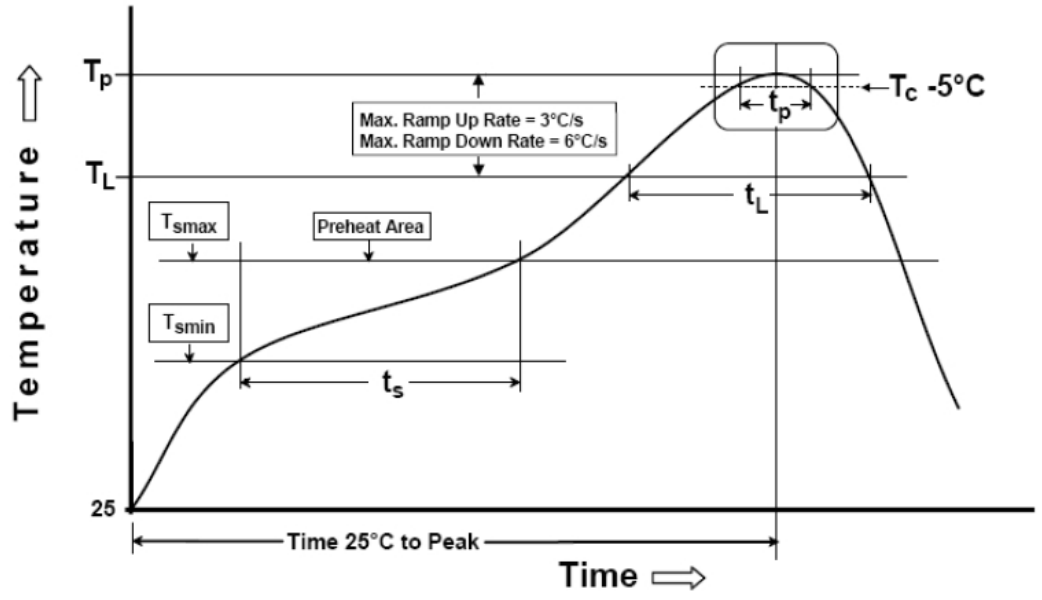


Fig 11 Furnace temperature curve

Note:

1. The maximum furnace temperature of the module is 260℃, don't exceed this temperature.

2. The gold plating thickness of the module pad is 2u".

12 Revision History

Revision	Release Date	Summary	Revised By
V1.0	2022-1-18	First release	yuangs